REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed September 20, 2002. Reconsideration and allowance of the application and presently pending claims, as amended, are respectfully requested.

Upon entry of the amendments in this response, claims 1-7, 10-16, 19-22, 25, and 27-29 remain pending in the present application. More specifically, claims 1, 4-6, 10, 11, 14, 16, 19-22, and 25 are directly amended; claims 17, 18, 23, 24, and 26 are canceled without prejudice, waiver, or disclaimer; and claims 27-29 are added.

Response To Claim Rejections Under 35 U.S.C. §102

Claims 1-4 and 11-13 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Yamane et al.* (U.S. Patent No. 4,965,797). Applicants respectfully traverse this rejection on the grounds that independent claims 1 and 11, as amended, contain patentable subject matter that is neither taught nor suggested by *Yamane et al.* Also, Applicants contend that the other cited references do not teach or suggest all of the claimed elements of independent claims 1 and 11.

Claim 1:

Independent claim 1 recites ***"a clock generating circuit configured to generate a master clock signal, a DCE clocking signal, and an internal clocking signal."*** Examples of clock generating circuits are shown in Figs. 4 and 5 of the present application, in which the clock generating circuits are made up of the master clock, the clock generator, and the selector. *Yamane et al.* does not include a circuit or combination of elements that produces three clocking signals as claimed. More particularly, *Yamane et al.* does not teach or suggest generating a ***"DCE clocking signal."***

Furthermore, independent claim 1 includes a sample enable generator that generates a first enable signal ***"at a first time"*** and a second enable signal ***"at a second time, the second time being subsequent to the first time."*** This aspect in claim 1 contrasts with elements and functions of *Yamane et al.* *Yamane et al.* does not disclose a sample enable generator as claimed, but instead discloses a control circuit 28 that

contains a D-type flip-flop. The outputs of the flip-flop are complementary outputs SEL1 and SEL2 that are produced simultaneously, as is well-known in the art of logic circuitry. Therefore, there is no teaching or suggestion in *Yamane et al.*, nor is there any motivation from the prior art, that would lead one of ordinary skill in the art to modify the flip-flop of *Yamane et al.* to produce output SEL1 at ***"a first time"*** and output SEL2 at a ***"second time, the second time being subsequent to the first time,"*** as is claimed in claim 1.

In addition, claim 1 also contains a sample comparator that is patentably distinguishable over the device of *Yamane et al.* Firstly, *Yamane et al.* does not disclose a ***"sample comparator,"*** which, as the name suggests, compares samples. Instead, *Yamane et al.* has a multiplexing circuit with logic components. The sample comparator, as defined in claim 1, is configured to ***"sample the DTE data signal at the first time and sample the DTE data signal at the second time."*** Although the multiplexing circuit of *Yamane et al.* receives data signals, there is no teaching or suggestion in *Yamane et al.* that a DTE data signal is sampled at a first time and sampled again at a second time subsequent to the first time.

The sample comparator is further distinguishable from *Yamane et al.* because it is configured to ***"compare the DTE data signal sampled at the first time with the DTE data signal sampled at the second time."*** Again, *Yamane et al.* does not compare a signal at a first time with the same signal at a later time.

To further distinguish the features of independent claim 1 from *Yamane et al.*, Applicants respectfully point out that the sample comparator is also configured to ***"determine, from the comparison, whether the DTE data signal has undergone a transition during the time interval between said first time and said second time."*** *Yamane et al.*, first of all, does not compare a signal at two different times, as mentioned above. Not only does *Yamane et al.* fail to compare samples, but *Yamane et al.* also fails to determine whether a ***"DTE data signal has undergone a transition during the time interval between said first time and said second time."***

Thus, the cited reference does not disclose, teach, or suggest all of the elements of independent claim 1. A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore &*

Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, it would be improper to maintain a rejection under 35 U.S.C. 102(b).

Claims 2-4 are believed to be allowable for at least the reason that these claims depend, directly or indirectly, from allowable independent claim 1. *In re Fine*, 837 F.2d 1071, 5 USPQ 2d 1596-1600 (Fed. Cir. 1988).

Claim 11:

Like claim 1, independent claim 11, as amended, also contains several elements that are not taught or suggested by *Yamane et al.* For example, claim 11 includes the step of ***"deriving a DCE clocking signal and an internal clocking signal from said master clock signal."*** This claimed feature is shown in Figs. 4 and 5 and described in the corresponding portions of the specification. For instance, the clock generator and selector of Figs. 4 and 5 provide the DCE clocking signal and the internal clocking signal. *Yamane et al.* does not disclose deriving two clocking signals from a master clock signal.

In addition, claim 11 includes the step of ***"obtaining a first sample of said DTE data signal at a first time and a second sample of said DTE data signal at a second time, said second time being subsequent to said first time."*** As mentioned above, *Yamane et al.* does not obtain samples of the same signal at two different times. Instead, *Yamane et al.* inputs two data signals at the same time.

As also mentioned above, the *Yamane et al.* reference further fails to teach or suggest the step of ***"comparing said first sample to said second sample,"*** as claimed. *Yamane et al.* does not compare samples, and, more particularly, does not compare samples of the same signal sampled at two different times.

It logically follows that, since *Yamane et al.* does not obtain samples of the same signal at two different times and compare the samples, it would be impossible for *Yamane et al.* to teach or suggest the step of ***"determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time,"*** as claimed in claim 11.

To maintain a rejection of a claim as being anticipated under 35 U.S.C. §102, all the elements of the claim must be disclosed in one reference. Anticipation requires that

each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.,* 976 F.2d 1559, 24 USPQ 2d 1321 (Fed. Cir. 1992). Thus, claim 11 is not anticipated by *Yamane et al.* for at least the reasons stated above.

Claims 12 and 13 are believed to be allowable for at least the reason that these claims depend, directly or indirectly, from allowable independent claim 11. *In re Fine, supra.*

Claims 6, 7, and 10:

Claims 6, 7, and 10 stand rejected under 35 U.S.C. §102 as being anticipated by *McMahan et al.* Applicants respectfully traverse this rejection on the grounds that *McMahan et al.* does not disclose all of the claimed features of independent claim 6, as amended.

For example, claim 6 now recites ***"means for deriving a circuit clocking signal from said master clock signal."*** *McMahan et al.* does not teach or suggest deriving a clocking signal from the master clock signal. Instead, the TX clock generator 55 of *McMahan et al.* receives an input indicating which phase of a TX clock is to be generated. The TX clock generator 55 does not include ***"means for deriving a circuit clocking signal from said master clock signal."*** No deriving function is taught or suggested by *McMahan et al.* More particularly, *McMahan et al.* does not teach deriving a clocking signal that has ***"the same frequency as the DCE clocking signal,"*** as claimed in claim 6.

For clarification, the circuit clocking signal can be seen in Figs. 4 and 5. For example, in Fig. 4, the circuit clocking signal, derived from the master clock signal by the clock generator, is DCE ST that is output at 25 and sent to the selector via connection 39. In Fig. 5, the circuit clocking signal is inverted by 44 and output as SD LATCH CLK on 24. Also, this circuit clocking signal is input into selector via connection 39.

Furthermore, claim 6 contains ***"means for inverting said circuit clocking signal."*** For clarification, this aspect can be seen, for example, in Figs. 4 and 5 where the

circuit clocking signal in inverted by inverter 41. *McMahan et al.* does not teach or suggest inverting the circuit clocking signal.

Claim 6 also includes ***"means for selecting, in response to said selector control signal, an output signal from the group consisting of said circuit clocking signal and said inverted clocking signal."*** Since the circuit clocking signal is not inverted in *McMahan et al.*, as mentioned above, it also follows that a selection of two clocking signals, one including the inverted clocking signal that does not exist in *McMahan et al.*, could not be done in *McMahan et al.*

Thus, independent claim 6 is not anticipated by *McMahan et al.* and Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. §102. Dependent claims 7 and 10 are likewise allowable for at least the reason that they depend from allowable independent claim 6. *In re Fine, supra.*

New Claims

Claims 27-29 have been newly added to further define and/or clarify the scope of the invention. Claims 27 and 28 include the components of the clocking generating circuit. The clock generating circuit comprises a clock generator, inverter, and a selector that selects either the generated clock signal or the inverted clock signal. *Yamane et al.* does not teach or suggest these details. Claim 29 is presented as the alternative embodiment (FIG. 5) such that the DCE clocking signal is selected from the internal clocking signal or the inverted clocking signal. This claim too is allowable over the reference to *Yamane et al.* since the reference does not teach or suggest producing a DCE clocking signal by a selection of two inverse clocking signals.

Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-7, 10-16, 19-22, 25, and 27-29 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231, on December 5, 2002.

Evelyn J. Sanders
Signature -

MARKED-UP VERSION OF AMENDED CLAIMS

The following is a marked-up version of the amended claims in which added language is underlined and deleted language is enclosed within brackets.

1. (Three Times Amended) A circuit for detecting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

[a master clock producing] a clock generating circuit configured to generate a master clock signal, [having a frequency that is an integer multiple of the frequency of the DCE clocking signal;

a clock generator deriving] a [circuit] DCE clocking signal, [from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal] and an internal clocking signal, each of the DCE clocking signal and internal clocking signal having a first frequency that is a fraction of the frequency of the master clock signal;

a sample enable generator configured to receive the master clock signal and the internal clocking signal and to generate [for generating] a first sample enable signal at a first time [related to said circuit clocking signal] and a second sample enable signal at a second time [related to said master clock signal], the second time being subsequent to the first time; and

a sample comparator [for using] having inputs that receive said first sample enable signal, said second enable signal and said DTE data signal, the sample comparator configured to sample the DTE data signal at the first time and sample the DTE data signal at the second time, the sample comparator further configured to compare the DTE data signal sample at the first time with the DTE data signal sampled at the second time and determine, from the comparison, whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

4. (Once Amended) The circuit of claim 1, wherein said sample comparator generates a selector control signal [if said first sample is different from said second sample] when the sample comparator determines that the DTE data signal has undergone a transition.

5. (Once Amended) The circuit of claim 4, [further comprising] wherein the clock generating circuit comprises:

a clock generator that generates the DCE clocking signal;

an inverter [producing] that produces an inverted [circuit] DCE clocking signal from said [circuit] DCE clocking signal; and

a selector [producing an output signal] that receives the DCE clocking signal and the inverted DCE clocking signal and produces the internal clocking signal that is selected, in response to the selector control signal, from the group consisting of said [circuit] DCE clocking signal and said inverted [circuit] DCE clocking signal [, in response to said selector control signal].

6. (Three Times Amended). A circuit for detecting and correcting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal [having a frequency greater than the frequency of the DCE clocking signal];

means for deriving a [circuit] DCE clocking signal and an internal clocking signal from said master clock signal, said [circuit] internal clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and [means for] obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal;

means for comparing said first sample to said second sample;

means for generating a selector control signal if said first sample is different from said second sample;

means for inverting said [circuit] internal clocking signal to produce an inverted [circuit] clocking signal; and

means for selecting, in response to said selector control signal, an output signal from the group consisting of said [circuit] internal clocking signal and said inverted [circuit] clocking signal.

10. (Three Times Amended) The circuit of claim 6, further comprising:

means for latching said DTE data signal, the means for latching being clocked by said internal clocking signal.

11. (Three Times Amended). A method for detecting clocking errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal [having a frequency that is an integer multiple of the frequency of the DCE clocking signal];

deriving a [circuit] DCE clocking signal and an internal clocking signal from said master clock signal, said [circuit] internal clocking signal having the same frequency as the DCE clocking signal;

obtaining a first sample of said DTE data signal at a first time [based on said circuit clocking signal] and a second sample of said DTE data signal at a second time [based on said master clock signal], said second time being subsequent to said first time, the time interval between said first time and said second time being less than the period of the DCE clocking signal; [and]

comparing said first sample to said second sample; and

determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time.

14. (Twice Amended) The method of claim 13, further comprising the steps of:

inverting said [circuit] DCE clocking signal to produce an inverted [circuit] clocking signal; and

producing [an output] said internal clocking signal that is selected, in response to said selector control signal, from the group consisting of said [circuit] DCE clocking signal and said inverted [circuit] clocking signal [, in response to said selector control signal].

16. (Once Amended) The circuit of claim 5, further comprising:

a data latch, clocked by said internal clocking signal, for latching said DTE data signal.

19. (Once Amended) The circuit of claim [17] 16, wherein said first enable signal is generated on the rising edge of said output signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

20. (Once Amended) The circuit of claim [17] 16, wherein said first enable signal is generated one master clock period before the rising edge of said [output] internal clocking signal and said second enable signal is generated one master clock period after [said first enable signal] the rising edge of said internal clocking signal.

21. (Once Amended) The circuit of claim [18] 28, wherein said first enable signal is generated on the rising edge of said [circuit] internal clocking signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

22. (Once Amended) The circuit of claim [18] 28, wherein said first enable signal is generated one master clock period before the rising edge of said [circuit] internal clocking signal and said second enable signal is generated one master clock period after [said first enable signal] the rising edge of said internal clocking signal.

25. (Once Amended) The method of claim 15, further comprising the [steps] step of:

[using said output signal as said the DCE clocking signal; and]

performing said obtaining step and said latching step according to a time sequence referenced to said [circuit] internal clocking signal.